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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/486,556	02/29/2000	NOBUAKI HASHIMOTO	105029	8629

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EXAMINER

PATEL, ISHWARBHAI B

ART UNIT PAPER NUMBER

2827

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/486,556

Applicant(s)

HASHIMOTO, NOBUAKI

Examiner

Ishwar (I. B.) Patel

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 June 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 30-85 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 30-85 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. Pre amendment filed on June 6, 2002 in this suspended continued prosecution application has been entered and prosecution has been reopened. The allowance of September 9, 2002 has been withdrawn, as the pre amendment, paper No. 17, was not timely matched.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 68-71, 73-77, 79 and 82-85 are rejected under 35 U.S.C. 102(e) as being anticipated by Imasu et al., US Patent No. 6,208,525, hereafter Imasu.

Regarding claim 68, 82 and 84, Imasu discloses a semiconductor device,  
comprising:

a substrate (wiring board 1, see figure 1 and 2 and 11, column 4, line 1-25),

said substrate having an interconnect pattern formed there over (see figure 2 and  
11),

said substrate having a protective layer covering at least a part of said  
interconnect pattern (passivation film 5 and 6, see figure 2 and 11, column 4, line 40-  
50);

a semiconductor chip said semiconductor chip having electrodes, said electrodes  
electrically connected to said interconnect pattern, said semiconductor chip mounted on  
said substrate such that an edge of said semiconductor chip does not overlap with said  
protective layer (semiconductor chip 10, see figure 2 and 11); and

an adhesive, said adhesive adhering said semiconductor chip to said substrate,  
said adhesive provided on said substrate from a region in which said semiconductor  
chip is mounted to said protective layer (adhesive 16, see figure 2 and 11, column 4,  
line 55-60).

Regarding claim 74, 83 and 85, Imasu discloses all the features of the claimed invention as applied to claim 68 above including adhesive the part of interconnect pattern below edge portion, see figure 2, 11).

Regarding claim 69 and 75, Imasu further discloses an anisotropic adhesive (column 8, line 1-10).

Regarding claim 70 and 76, Imasu further discloses anisotropic conductive cover whole of said interconnect pattern (figure 2 and 11).

Regarding claim 71 and 77, Imasu further discloses the adhesive covering part of a lateral surface of said semiconductor chip (see figure 2 and 11).

Regarding claim 73 and 79, Imasu further discloses the protective layer cover said substrate except said region in which said semiconductor chip is mounted and a periphery of said region (passivation film 5 and 6, see figure 2 and 11, column 4, line 40-50).

4. Claims 72 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imasu et al., US Patent No. 6,208,525, hereafter Imasu, as applied to claims 68-71, 73 and 74 to 77 and 79 above, and further in view of Shigeki, Japanese Patent JP356050546A.

Regarding claims 72 and 78, the applicant is claiming a shading material added to the adhesive. Though, Imasu does not disclose such shading, shading is known in the art and can be used depending upon the specific requirement for shielding the semiconductor die from light rays. Shigeki disclose discloses such light shielding resin for protecting the chip from malfunctioning and damage. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the assembly of Imasu with shading material added in the adhesive in order to shielding the chip from light. Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

5. Claims 30-67, 80-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imasu et al., US Patent No. 6,208,525, hereafter Imasu and Shigeki, Japanese Patent JP356050546A, as applied to claims 68-79 above and Higashi et al., US Patent 5,918,113, here after Higashi.

Regarding claims 30-67, the applicant is claiming the method of manufacturing a semiconductor device. The combination of Imasu and Shigeki discloses the all the limitation of the product as claimed and the method steps are inherent and obvious, if not identical, in view of the product claims.

Regarding claim 80 and 81, the applicant is claiming the semiconductor devices by the method as defined in claims 30 and 50, respectively. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentability distinguish the product over the prior art, in the case that the product is the same or obvious over, the prior art, See Product-by-Process in MPEP 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

### ***Double Patenting***

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 30 – 85 are rejected under the judicially created doctrine of double patenting over claims 1-29 of U. S. Patent No. 6,462,284 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming

common subject matter, as follows: The present application and the patent both claims the method of installing a semiconductor die on a substrate using conductive adhesive and the though not identical in language, they are obvious. Further, both the applications claim priority against the Japanese application (JP) 10-201246, July 1, 1998.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application, which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

### ***Conclusion***

8. Applicant's arguments with respect to the newly added claims 30-85 have been considered but are moot in view of the new ground(s) of rejection.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Higashi and Watanabe disclose a process for producing a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers




Art Unit: 2827

for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp  
October 22, 2002

  
**ALBERT W. PALADINI**  
**PRIMARY EXAMINER**

  
**DAVID L. TALBOTT**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**